SEMICONDUCTOR DEVICE WITH ASYMMETRIC POCKET IMPLANTS

FIELD OF THE INVENTION

[0001] The present invention relates to a semiconductor device with a single deep-pocket ion implant and a single shallow-pocket ion implant to counter short channel effects, SCE.

BACKGROUND OF THE INVENTION

[0002] US patent 6,344,405 discloses a semiconductor device that comprises, a source, an oxide-supported gate and a drain, which extend lengthwise along a substrate. The device requires a threshold voltage V_t to turn on the device, from a nonconductive, off state. Leakage currents near the source and drain tend to occur within a source depletion region and a drain depletion region. These depletion regions are in the substrate beneath the oxide-supported gate, and between the source and the drain. The source and drain depletion regions electrically couple to the transistor source and the transistor drain, respectively, which contributes to leakage current.

[0003] When the length of the gate, L_{gate}, is made desirably smaller, for example, when L_{gate} decreases below 0.1 μm (micrometers), these depletion areas have a tendency for electrically coupling to each other, which increases the likelihood of a leakage current between the source and the drain. Such an electrical coupling, as L_{gate} decreases, is referred to as, a short channel effect (SCE), or alternatively as, a punch through effect.

SUMMARY OF THE INVENTION

[0004] The present invention counters the punch through effect or SCE by providing a semiconductor device having a deep-pocket ion implant in a deep source-drain depletion region, and further having a shallow-pocket ion implant in a shallow source-drain depletion region. Various embodiments of the present invention counter variations in the punch through effect or SCE by having implants in different locations.

Another embodiment of the present invention resides in a method of fabricating a semiconductor device to counter the punch through effect or SCE.

[0005] Embodiments of the present invention will now be described by way of example with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is a schematic view of an embodiment of a semiconductor device having shallow and deep pocket ion implants at a drain side of the semiconductor device.

[0007] FIG. 2 is a schematic view of an embodiment of a semiconductor device having shallow and deep pocket ion implants at a source side of the semiconductor device.

[0008] FIG. 3 is a schematic view of an embodiment of a semiconductor device having shallow and deep pocket ion implants, respectively, at a source side and a drain side of the semiconductor device.

[0009] FIG. 4 is a schematic view of another embodiment of a semiconductor device having shallow and deep pocket ion implants, respectively, at a drain side and a source side, respectively, of the semiconductor device.

[0010] FIG. 5 is a schematic view of a lightly doped drain implant process step.

[0011] FIG. 6 is a schematic view of a tilted pocket implant process step to produce first and second ion implants.

[0012] FIG 7 is a schematic view of a Si_3N_4 process step and an SiO_2 process step.

[0013] FIG 8 is a schematic view of two process steps providing spacers on a semiconductor device.

[0014] FIG. 9 is a schematic view of a process step of deep source-drain implantation and a process step of rapid thermal annealing to provide an asymmetric ion implant when the ion strength concentration of a second ion implant is countered.

[0015] FIG. 10 is a schematic view of the process step of Fig. 5 applied to the embodiment of Fig. 4.

[0016] FIG. 11 is a schematic view of the process step of Fig. 6 applied to the embodiment of Fig. 4.

[0017] FIG. 12 is a schematic view of the process step of Fig. 6 applied a second time to the embodiment of Fig. 4.

[0018] FIG. 13 is a schematic view of the two process steps of Fig. 7 applied to the embodiment of Fig. 4.

[0019] FIG. 14 is a schematic view of the two process steps of Fig. 8 applied to the embodiment of Fig. 4.

[0020] FIG. 15 is a schematic view of the two process steps of Fig. 9 applied to the embodiment of Fig. 4.

[0021] FIG. 16 is a schematic view of the process step of Fig. 5 applied to the embodiment of Fig. 3.

[0022] FIG. 17 is a schematic view of the process step of Fig. 6 applied to the embodiment of Fig. 3.

[0023] FIG. 18 is a schematic view of the process step of Fig. 6 applied a second time to the embodiment of Fig. 3.

[0024] FIG. 19 is a schematic view of the two process steps of Fig. 7 applied to the embodiment of Fig. 3.

[0025] FIG. 20 is a schematic view of the two process steps of Fig. 8 applied to the embodiment of Fig. 3.

[0026] FIG. 21 is a schematic view of the two process steps of Fig. 9 applied to the embodiment of Fig. 3.

[0027] FIG. 22 is a schematic view of the process step of Fig. 5 applied to the embodiment of Fig. 1.

[0028] FIG. 23 is a schematic view of the process step of Fig. 6 applied to the embodiment of Fig. 1.

[0029] FIG. 24 is a schematic view of the process step of Fig. 6 applied a second time to the embodiment of Fig. 1.

[0030] FIG. 25 is a schematic view of the two process steps of Fig. 7 applied to the embodiment of Fig. 1.

[0031] FIG. 26 is a schematic view of the two process steps of Fig. 8 applied to the embodiment of Fig. 1.

[0032] FIG. 27 is a schematic view of the two process steps of Fig. 9 applied to the embodiment of Fig. 1.

[0033] FIG. 28 is a schematic view of the process step of Fig. 5 applied to the embodiment of Fig. 2.

[0034] FIG. 29 is a schematic view of the process step of Fig. 6 applied to the embodiment of Fig. 2.

[0035] FIG. 30 is a schematic view of the process step of Fig. 6 applied a second time to the embodiment of Fig. 2.

[0036] FIG. 31 is a schematic view of the two process steps of Fig. 7 applied to the embodiment of Fig. 2.

[0037] FIG. 32 is a schematic view of the two process steps of Fig. 8 applied to the embodiment of Fig. 2.

[0038] FIG. 33 is a schematic view of the two process steps of Fig. 9 applied to the embodiment of Fig. 2.

[0039] FIG. 34 is a schematic view of a semiconductor device having two sets of symmetric ion implants.

[0040] FIG. 35 is a graph of device performance compared with performance of a device having symmetric halo implants.

[0041] FIG. 35 is a graph indicating SCE or punch through effect on device performance as a function of gate length.

DETAILED DESCRIPTION

[0042] With reference to Fig. 1, an embodiment of the present invention, which is indicated as Dd, resides in a semiconductor device 1 comprising: a source 2 , an oxide-supported gate 3, supported on a film of oxide 3a, and a drain 4, all of which are supported lengthwise on a semiconducting substrate 5.

[0043] The source 2 includes a shallow source extension 2a and a deep source portion 2b in a source-drain region. The drain 4 includes a shallow drain extension 4a

and a deep drain portion 4b in the source-drain region. The source-drain region is in the substrate 5 under the gate 3. The source-drain region extends lengthwise to include the source 3 and the drain 4. The source-drain region has a shallow source-drain region between the source extension 2a and the drain extension 4a. The source-drain region has a deep source-drain region between the deep source portion 3a and the deep drain portion 4a. For example, the semiconductor device 1 is a field effect transistor, FET. An FET comprises either a PMOSFET, a p-type metal oxide silicon field effect transistor, or an NMOSFET, an n-type metal oxide silicon field effect transistor.

[0044] The semiconductor device 1 has a source depletion region 6. The source depletion region 6 includes a shallow source depletion region 6a and a deep source depletion region 6b. The semiconductor device 1 has a drain depletion region 7. The drain depletion region 7 includes a shallow drain depletion region 7a and a deep drain depletion region 7b. The source-drain depletion region is between the source 3 and the drain 4. The source-drain depletion region is in the substrate 5 under the gate 3, and is where the SCE or punch through effect can occur.

[0045] With further reference to Fig. 1, asymmetric pocket implants are provided to counter the SCE or punch through effect. They are single pocket implants that are asymmetric relative to a vertical central axis of the semiconductor device 1, as viewed in Fig. 1. The semiconductor device 1 has a deep-pocket ion implant 8 in the deep source-drain depletion region. A shallow-pocket ion implant 9 is in the shallow source-drain depletion region. For a PMOSFET, both the deep-pocket ion implant 8 and the shallow-pocket ion implant 9 are N-doped with respective concentrations of N-doped ions. The respective concentrations of N-doped ions are either equal or different. For an NMOSFET, both the deep-pocket ion implant 8 and the shallow-pocket ion implant 9 are P-doped with respective concentrations of P-doped ions. The respective concentrations of P-doped ions are equal or different. The structure described above with reference to Fig. 1 applies similarly to each of the embodiments disclosed in Figs. 2-4.

[0046] The embodiment of Fig. 1 discloses the deep pocket implant 8 at the drain side, meaning, closer to the drain 4 than to the source 2. The deep pocket implant 8 at the

drain side is in the drain depletion region 7. The shallow pocket ion implant 9 is at the drain side, and in the drain depletion region 7.

[0047] Fig. 2 discloses another embodiment of the present invention that is indicated as Ss. With reference to Fig. 2, the deep-pocket ion implant 8 is at the source side, meaning closer to the source 2 than to the drain 4. The deep-pocket ion implant 8 is in the source depletion region 6. The shallow-pocket ion implant 9 is in the substrate 5 at the source side and in the source depletion region.

[0048] Fig. 3 discloses another embodiment of the present invention that is indicated as Sd. With reference to Fig. 3, the deep-pocket ion implant 8 is at the drain side, and in the drain depletion region 7. The shallow pocket implant 9 is at the source side, and in the source depletion region 6.

[0049] Fig. 4 discloses another embodiment that is indicated as sD in Fig. 4. With reference to Fig. 4, the deep pocket ion implant 8 is at the source side, and in the source depletion region 6. The shallow-pocket ion implant 9 is at the drain side, and in the drain depletion region 7.

[0050] Figs. 1-4 disclose the asymmetric deep pocket implant 8 and the asymmetric shallow pocket implant 9 in different locations to provide countering adjustments that counter the variations in the punch through effect or SCE.

[0051] With reference to Figs. 5-9, a process of sequential process steps will now be described for making a semiconductor device 1 with an asymmetric pocket implant. First, conventional process steps form the substrate 5, and an oxide film under the gate 3. Further conventional process steps form the gate 3.

[0052] Fig. 5 discloses a process step of lightly doped drain and source implantation. This process step is a shallow ion implantation at zero tilt angle. Implanted ion impurities form light doped source and drain regions of a transistor. For example implanted Arsenic, As, forms light doped source and drain regions for NMOS transistors.. Further, for example, Boron and/or Boron Fluoride, B and BF_2 , impurities form light doped source and drain regions for PMOS transistors. The impurities are implanted with a zero tilt angle. The impurities are impelled vertically along the vertical

vector 10 in Fig. 5. For example, the light doped source 2a and the light doped drain 4a are formed simultaneously by the first process step.

[0053] Fig. 6 discloses a process step of deep pocket ion implantation at a tilt angle to form a set of two deep pocket ion implants 8. Implanted ion impurities are formed simultaneously in the substrate 5. The tilt angle is tilted toward the source side of the semiconductor device 1 to form a primary implant 8 at the source side of the semiconductor device 1, and form a secondary implant 8 at the drain side of the semiconductor device 1.

[0054] The primary implant 8 is formed under the gate 3 on either the source side or the drain side, depending on the direction of the tilt angle. Although not shown, the tilt angle can be tilted to form a drain side, primary implant 8, at the drain side of the semiconductor device 1, wherein such primary implant 8 is under the gate 3 at the drain side of the semiconductor device 1.

[0055] A secondary implant 8 is formed at the drain side of the semiconductor device. This secondary implant 8 will be countered by performance of such further process steps to be discussed with reference to Figs. 7-9. According to the invention, the primary implant 8 becomes a single ion implant and an asymmetric ion implant when the secondary implant 8 is countered.

[0056] A process step disclosed by Fig. 6 applies to implantation of either shallow or deep ion implants 8 or 9, depending on the strength of the implantation energy to impel the implants either shallow or deep, and further depending on the ion concentrations that dissipate the implantation energy. Further, the tilt of the implant angle from shallow (larger tilt angle) to steep (smaller tilt angle) affects the implant depth from shallow to deep, respectively.

[0057] The process step of Fig. 6 is capable of being repeated to form another set of primary and secondary shallow-pocket ion implants 9. For example, the process of Fig. 6 can be repeated to form a set of two shallow ion implants 9, to be further disclosed by Fig. 12.

[0058] Fig. 7 discloses a first process step of forming a thin layer 11 of SiO_2 an insulating barrier on the substrate 5 and on each gate 3 on the substrate. The thin layer 11

of SiO_2 is formed by TEOS (Tetraethoxysilane), by way of example. Another process step of forming a thicker layer 12 of Si_3N_4 on the insulating barrier covers the lateral sides of each gate 3. The layer 12 is formed by chemical vapor deposition, CVD, by way of example.

[0059] Fig. 8 discloses a process of forming spacers 13 of Si_3N_4 material against the lateral sides of each gate 3. The spacers 13 are formed by dry etching the layer of Si_3N_4 and the spacers 13 are against an insulating thin layer 11 of SiO_2 on the sides of the gate 3. Portions of SiO_2 material are uncovered by the spacers 13. A process step of wet dipping in an etchant of SiO_2 removes the uncovered SiO_2 material.

[0060] Fig. 9 discloses a process step of deep source-drain implantation at zero tilt angle. This process step is a deep ion implantation at zero tilt angle of highly doped ions. Implanted ion impurities form a deep source portion 2b and a deep drain portion 4b. For example implanted Arsenic, As, forms implanted n+ source and n+ drain regions for NMOS transistors. Further, for example, Boron and/or Boron Fluoride, B and BF_2, impurities form implanted p+ source and p+ drain regions for PMOS transistors.

[0061] With continued reference to Fig. 9, the gate 3 and the spacer 13 cover the source side, primary implant 8 while ions of the deep source portion 2b are impelled along the vector 10 of zero tilt angle. The drain side, secondary implant 8 is uncovered by the gate 3 and any spacer 13 while ions of the deep drain portion 4b are impelled along the vector 10 of zero tilt angle. Thus the ions of the deep drain portion 4b are combined with the uncovered secondary implant 8 in the space occupied by the uncovered secondary implant 8. The doped polarity of the source 2 and drain 4, including the portions 2a, 2b, 4a and 4b, are opposite the doped polarity of the implants 8. For example, an Arsenic ion of the deep drain portion 4b has more free electrons than the single electron receptor of a Boron ion of the uncovered secondary implant 8. Thus, the polarity of the Boron ions in the secondary implant 8 is neutralized by the Arsenic ions. Further, the secondary implant 8 is surrounded by the ion distribution of the deep drain portion 4b. The secondary implant 8 is said to be countered by counter doped implanted ions of the deep drain portion 4b. Thus, the source side, primary implant 8 becomes an

asymmetric ion implant, when the drain side, secondary implant 8 is countered by counter doped implanted ions.

[0062] With continued reference, to Fig. 9, a process step of rapid thermal annealing of the semiconductor device 1 is performed, to refine the crystalline structure and repair structural damage caused by ion implantation. Annealing causes joining of the source extension 2a and the deep source 2. Annealing further causes joining of the drain extension 4a and the deep drain 4.

[0063] Figs. 10-15 disclose how the process steps of Figs. 5-9 apply to make the embodiment sD disclosed in Fig 4. Fig. 10 discloses a light doped source 2a and a light doped drain 4a made by performing the process step disclosed by Fig. 5.

[0064] Fig. 11 discloses a deep pocket primary implant 8 formed by performing the process step of Fig. 6, with a tilt angle tilted to the source side of the semiconductor device 1. Fig. 11 discloses a deep pocket secondary implant 8 that is countered by ion implants to be further disclosed by Fig. 15.

[0065] Fig. 12 discloses a drain side, shallow pocket primary implant 9 and a shallow pocket secondary implant 9 formed by performing the process step of Fig. 6, by having the tilt angle tilted toward the drain side of the semiconductor device 1. The primary implant 9 is under the gate 3.

[0066] Fig. 13 discloses a thin layer of SiO_2 and a thicker layer of Si_3N_4 formed by performing the two process steps disclosed by Fig. 7.

[0067] Fig. 14 discloses spacers 13 formed by the two process steps disclosed by Fig. 8.

[0068] Fig. 15 discloses a deep source portion 2b and a deep drain portion 4b formed by the process step disclosed by Fig. 9. In Fig. 15, the source side, deep primary implant 8 and the drain side, shallow primary implant 9 become asymmetric ion implants, respectively, when the secondary implant 8 and the secondary implant 9 are countered. Then a process of rapid thermal annealing of the semiconductor device 1 is performed as disclosed by Fig. 9.

[0069] Figs. 16-21 disclose how the process steps of Figs. 5-9 apply to make the embodiment Sd disclosed by Fig. 3. Fig. 16 discloses a light doped source 2a and a light doped drain 4a made by performing the process step disclosed by Fig. 5.

[0070] Fig. 17 discloses a drain side, deep pocket primary implant 8 formed by performing the process step of Fig. 6, with a tilt angle tilted to the drain side of the semiconductor device 1. Fig. 17 discloses a deep pocket secondary implant 8 that is countered by ion implants to be disclosed by Fig. 21.

[0071] Fig. 18 discloses a source side, shallow-pocket primary implant 9 and a drain side, shallow-pocket secondary implant 9 formed by performing the process step of Fig. 6, with the tilt angle tilted toward the source side of the semiconductor device 1. The primary implant 9 is under the gate 3 at the source side of the semiconductor device 1.

[0072] Fig. 19 discloses a thin layer of SiO_2 and a thicker layer of Si_3N_4 formed by the two process steps disclosed by Fig. 7.

[0073] Fig. 20 discloses spacers 13 formed by the two process steps disclosed by Fig. 8.

[0074] Fig. 21 discloses a deep source portion 2b and a deep drain portion 4b formed by the process disclosed by Fig. 9. In Fig. 21, the drain side, deep primary implant 8 and the source side, shallow primary implant 9 become asymmetric ion implants, respectively, when the secondary implant 8 and the secondary implant 9 are countered. Then a process of rapid thermal annealing of the semiconductor device 1 is performed as disclosed by Fig. 9.

[0075] Figs. 22-27 disclose how to make the embodiment Dd disclosed by Fig. 1. Fig. 22 discloses a shallow source extension 2a and a shallow drain extension 4a made by performing the process step disclosed by Fig. 5.

[0076] Fig. 23 discloses a drain side, deep pocket primary implant 8 formed by performing the process step of Fig. 6, with a tilt angle tilted to the drain side of the semiconductor device 1. Fig. 23 discloses a deep pocket secondary implant 8 that is countered by ion implants to be disclosed by Fig. 27.

[0077] Fig. 24 discloses a drain side, shallow pocket primary implant 9 and a shallow pocket secondary implant 9 formed by performing the process step of Fig. 6, by

having the tilt angle tilted toward the drain side of the semiconductor device 1. The drain side, primary implant 9 is under the gate 3 at the drain side of the semiconductor device 1.

[0078] Fig. 25 discloses a thin layer of SiO_2 and a thicker layer of Si_3N_4 formed by the two process steps disclosed by Fig. 7.

[0079] Fig. 26 discloses spacers 13 formed by the two process steps disclosed by Fig. 8.

[0080] Fig. 27 discloses a deep source portion 2b and a deep drain portion 4b formed by the process disclosed by Fig. 9. In Fig. 27, the drain side primary deep implant 8 and the drain side primary shallow implant 9 become asymmetric ion implants, respectively, when the deep secondary implant 8 and the shallow secondary implant 9 are countered. Then a process of rapid thermal annealing of the semiconductor device 1 is performed, as disclosed by Fig. 9.

[0081] Figs. 28-33 disclose how the process steps of Figs. 5-9 apply to make the embodiment Ss as disclosed by Fig. 2. Fig. 28 discloses a light doped source 2a and a light doped drain 4a made by performing the process step disclosed by Fig. 5.

[0082] Fig. 29 discloses a source side, deep pocket primary implant 8 formed by performing the process step of Fig. 6, with a tilt angle tilted to the source side of the semiconductor device 1. Fig. 29 discloses a deep pocket secondary implant 8 that is countered by ion implants to be disclosed by Fig. 33.

[0083] Fig. 30 discloses a source side, shallow pocket primary implant 9 and a shallow pocket secondary implant 9 formed by performing the process step of Fig. 6, by having the tilt angle tilted toward the source side of the semiconductor device 1. The source side, primary implant 8 is under the gate 3 at the source side of the semiconductor device 1.

[0084] Fig. 31 discloses a thin layer of SiO_2 and a thicker layer of Si_3N_4 formed by the two process steps disclosed by Fig. 7.

[0085] Fig. 32 discloses spacers 13 formed by the two process steps disclosed by Fig. 8.

[0086] Fig. 33 discloses a deep source portion 2b and a deep drain portion 4b formed by the process disclosed by Fig. 9. In Fig. 33, the source side, deep primary implant 8 and the source side, shallow primary implant 9 become asymmetric ion implants, respectively, when the deep secondary implant 8 and the shallow secondary implant 9 are countered. Then a process of rapid thermal annealing of the semiconductor device 1 is performed as disclosed by Fig. 9.

[0087] Fig. 34 discloses an embodiment SD of a semiconductor device 1 with a set of two deep-pocket primary implants 8, and a set of two shallow-pocket primary implants 9. Further, the implants are known as, symmetric halo implants, meaning that they are imbedded at the same level, and further, they are symmetrically spaced apart. The embodiment SD is manufactured with symmetric halo implants as proposed by US 6344405 and FR 2796204.

[0088] According to each of the embodiments disclosed in Figs. 1-4, the shallow-pocket ion implant 9 has both, a smaller size and a heavier ion dose, in contrast to the deep-pocket ion implant 8 having a larger size and smaller dose of ions. The shallow-pocket ion implant 9 is implanted by a lower level of implanting energy, in contrast to the deep-pocket ion implant 8 being implanted by a higher level of implanting energy. For a PMOSFET, the deep-pocket ion implant 8 is doped with Arsenic (As) impurity. Each of the embodiments disclosed by Figs. 1-4 are manufactured with ion implants 8 and 9 according to the following Table. The Table further discloses the device of Fig. 34 manufactured with symmetric halo implants.

Table I

Embodiment/pocket	Implant Energy (KeV)	Implant Dose (10^{13} cm^{-2})	Tilt Angle From Vertical (Degrees)
Dd/ deep-pocket	30	1.0	15
Dd/ shallow pocket	20	1.2	30
Ss/ deep-pocket	30	1.0	15
Ss/ shallow pocket	20	1.2	30
Sd/ deep-pocket	30	1.0	15
Sd/ shallow pocket	20	1.5	30
sD/ deep-pocket	30	1.0	15
sD/ shallow pocket	20	1.5	30
SD/ deep-pocket	30	1.5	15
SD/ shallow pocket	20	2.5	30

[0089] Fig. 35 discloses device performance of each of the embodiments Dd, Ss, Sd and sD of Figs. 1-4, as compared with the device performance of the device SD of Fig. 34., wherein device stand-by current I_{off} in nano-Amps per micrometer is plotted against device driving current I_{dsat} in micro-Amps per micrometer.

[0090] Fig. 36 discloses the SCE or punch through effect on device performance as a function of gate length L_{gate} in nanometers. The SCE or punch through effect is indicated for each of the embodiments Dd, Ss, Sd and sD of Figs. 1-4, as compared with the device performance of the device SD of Fig. 34, wherein V_t roll-off, $V_{t,\,sat}$ in Volts is plotted against reductions in gate length.

[0091] As indicated by Figs. 35 and 36, symmetric halo implants of the embodiment SD are associated with the following drawbacks. They tend to increase the apparent sheet resistance of the source and the drain, which decreases the driving current, I_{dsat}, when the semiconductor is in a conducting state. Further, they tend to induce a parasitic junction capacitance at both the source-substrate junction and the drain-substrate

junction, which degrades the circuit impedance and signal transmission speed. Further, leakage current in the deletion area at both the source-substrate junction and the drain-substrate junction is increased by the presence of the halo implants, which increases lost power consumption and heat generation. Further, as gate length, L_{gate}, is desirably reduced to make a smaller device, the threshold voltage V_t correspondingly decreases, which is an undesired effect known as, V_t roll-off.

[0092] Symmetric halo implants are always confined to being in a symmetrical arrangement with respect to each other, and thereby, are unsuccessful in countering V_t roll-off. In contrast, the respective locations of the single asymmetric deep-pocket ion implant 8, and the single asymmetric shallow-pocket ion implant 9 of embodiments Dd, Ss, Sd and sD are chosen independently, which individually adjusts the locations of the pocket implants 8 and 9 to counter V_t roll-off. For example, Fig. 36 indicates that V_t roll-off is countered effectively by the embodiment sD, Fig. 4, of the present invention, wherein the deep-pocket ion implant 8 is at or near the source 2, and further wherein, the shallow-pocket ion implant 9 is at or near the drain 4.

[0093] The embodiments disclosed herein, as well as, further embodiments and modifications of the present invention, are intended to be covered by the spirit and scope of the appended claims.